PATENT ABSTRACTS OF JAPAN

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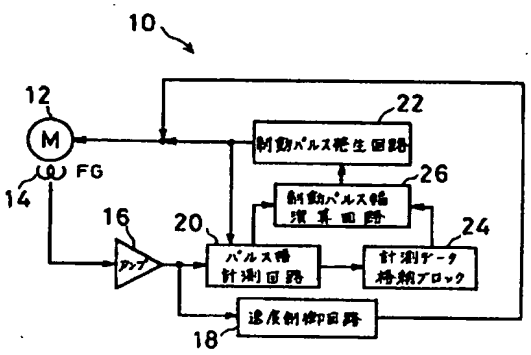
(54) D.C. MOTOR DAMPING CONTROL CIRCUIT

(57)Abstract:
PURPOSE: To achieve highly accurate control at a low cost by providing a computing means for calculating an predicted damping time of a d.c. motor and a damping pulse generating means.
CONSTITUTION: An FG pulse output from a frequency generator(FG) 14 is amplified by a amplifier 6, and input into a speed control circuit 18 and pulse width measurement circuit 20. The speed control circuit 18 outputs a speed control signal, and thereby controls a capstan motor 12 in conjunction with a damping pulse from a damping pulse generation circuit 22. The pulse width measurement circuit 20 is also fed with the damping pulse, and thus measures three sorts of pulse width data. Based on the frequency of a first FG pulse output from the pulse width measurement circuit 20 after the first transition of the damping pulse and that of a second FG pulse just before a measured data storage block 24, a damping pulse computation circuit 26 calculates a predicted damping time from a damping pulse being risen in at the damping pulse wide computation circuit 26 to the capstan motor 12 being stopped. The damping pulse generation circuit 22 make the damping pulse fall with accuracy based on the resultant predicted damping time.



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